REMARKS

Claims 1-13 and 15-16 are pending in this application. By this Amendment, claims 1-6, 9-11 and 13 are amended, claim 14 is canceled and claim 16 is added. Claims 1-6, 9-11 and 13 have been amended to correct informalities. In particular, "clock" has been changed to "clock signal" throughout the claims. The term "block" has been removed throughout the claims. The claims have further been amended to correct the typographical errors of the term media and medium. In particular, all claims are now similar to claim 1, which recites "at least one semiconductor storage medium including a plurality of semiconductor storage media." This change denotes a medium including a plurality of media, and provides consistency throughout the claims.

No new matter is added by this Amendment. Support for new claim 16 may be found in the original specification at, for example, paragraph [0029] and Fig. 1.

Rejections Relying on Haban, Hadji and Carter

Claims 1, 3-4, 6-9 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over "Haban" (U.S. Patent No. 6,779,125), in view of "Hadji" (U.S. Patent No. 6,079,024) in view of "Carter" (U.S. Patent No. 4,980,836). Applicant respectfully traverses this rejection.

The Patent Office alleges that Haban describes a bus master, a bus interface that controls access to at least one semiconductor storage medium based on a request for access to the at least one semiconductor storage medium from the bus master, and the at least one semiconductor storage medium including a plurality of semiconductor storage media.

Haban does not describe a single bus interface comprising a plurality of dedicated bus interfaces that each correspond to one of the semiconductor storage media as required by claim 1. Independent claims 4 and 9 recite similar subject matter.

The Patent Office alleges that Hadji remedies this deficiency of Haban. Applicant respectfully disagrees. Specifically, the Patent Office, on page 3, paragraph d of the Office Action, alleges that bus interface 108 of Hadji describes a bus interface including a plurality of dedicated bus interfaces that each correspond to one of the semiconductor storage mediums as required by claim 1. However, Fig. 2 of Hadji clearly shows that bus interface 10 contains within it four buffers 214, 216, 218 and 220, with buffers 214, 216, 218, and 220 all interfacing with a single, non-dedicated, data bus 101 (see Fig. 2 of Hadji).

Fig. 1 of the present application clearly shows a semiconductor device with a bus master, a clock-signal generator, a clock-supply-control circuit and a bus interface. According to claim 1, the bus interface includes a first dedicated bus interface and a second dedicated bus interface (see Fig. 1 of the application). The clock-supply-control circuit interfaces with each of the dedicated bus interfaces and the common bus interface. The first and the second dedicated bus interfaces interface directly with the SRAM and the SDRAM, respectively, of the semiconductor storage medium (see Fig. 1). Therefore, the clock-supply-control interfaces with the first dedicated bus interface and the second dedicated bus interface, which each interface with a dedicated storage media, respectively (see Fig. 1 of the application).

In contrast, Hadji shows, in Fig. 2 that the clock control 202 interfaces only with the clock unit 204. The clock unit 204 interfaces directly with each of the buffers 214, 216, 218, and 220. The buffers interface with the non-dedicated data bus 101. The bus interface 101 of Hadji may interface with the clock control unit 202, as shown in Fig. 3 of Hadji. However, Hadji does not show that the clock control unit 202 interfaces with a first dedicated bus interface or a second dedicated bus interface that each separately and individually interface with a dedicated media as shown in Fig. 1 of the application.

Furthermore, the Patent Office alleges that the buffers 214, 216, 218, and 220 of Hadji are interpreted as dedicated bus interfaces corresponding to a certain one of the storage media. The Patent Office alleges that buffers 214 and 216 of Hadji correspond to system memory 106. Hadji states that Buffer 214 receives data from the system memory 106 and that buffer 216 receives data from data bus 101 and outputs the data to system memory 106 (see col. 4, lines 4-12 of Hadji). However, Hadji also states that master peripheral 110 may initiate a bus cycle in which data is stored to buffer 216. Therefore, because buffer 216 interfaces with master peripheral 110 and system memory 106, it can not describe a first dedicated bus interface or a second dedicated bus interface that corresponds to a respective storage media as required by the present claims 1, 4 and 9.

Therefore, Hadji does not describe the features of the semiconductor device of claim 1, the semiconductor circuit of claim 4, or the method of controlling a clock-supply of claim 9. Thus, Hadji does not remedy the deficiencies of Haban.

The Patent Office further alleges Carter describes that clock signals are removed from each of the dedicated bus interfaces a predetermined time after each dedicated bus interface completes its access to its dedicated storage media as required in claim 1, and claims 4 and 9 that recite similar requirements. Applicant respectfully disagrees. Claim 1 of the pending application recites a first dedicated bus interface stopping to receive a clock signal a predetermined time after access to its dedicated storage media and a second dedicated bus interface stopping to receive a clock signal a predetermined time after access to its dedicated storage media. Carter instead describes a single timer that monitors access to a hard disk unit, floppy disk unit, keyboard, serial ports and a printer to determine if the system is active. When inactivity in Carter is determined, the system is considered inactive and power is removed from the hard drive. Therefore, Carter does not describe the features recited in current claim 1, 4 or 9. Thus, Carter does not remedy the deficiencies of Haban and Hadji.

Further, there is no reason or rationale to have combined the teachings of Haban with those of Hadji and Carter, as Hadji already provides a method of stopping the clock signal to the data buffers. Even if one were to have combined the cited references, it would not have yielded all the features present in the current claims, as none of the cited references describe a first and a second dedicated bus interface corresponding to each of a plurality of storage media, as detailed above.

Thus, withdrawal of the rejection is respectfully requested.

Rejections Relying on Hadji, Micron and Carter

Claims 1, 3-4, 6-9 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Hadji in view of Micron High Performance SDRM Modules (hereinafter "Micron") in further view of Carter. Applicant respectfully traverses this rejection.

For at least the above reasons, applicant contends that Hadji does not describe the features of present claim 1, 4 or 9.

The Patent Office admits that Hadji does not describe a system memory comprising a plurality of semiconductor storage media. The Patent Office relies on Micron to overcome this deficiency alleging that Micron describes a memory module that may comprise a plurality of storage media. However, Micron does not remedy any of the deficiencies of Hadji detailed above.

The Patent Office again relies on Carter as allegedly describing that clock signals are removed from each of the dedicated bus interfaces a predetermined time after each dedicated bus interface completes its access to its dedicated storage media as required in claim 1, 4 and 9. However, for the reasons stated previously, Carter does not describe the features of claims 1, 4 and 9. Thus, Carter does not remedy the deficiencies of Hadji and Micron.

Withdrawal of the rejection is respectfully requested.

New Claim 16

New claim 16 is directed to the semiconductor device of claim 1, wherein the at least one semiconductor storage medium is externally located to the bus interface. As stated previously, Hadji describes a bus interface 108, that is shown to include data buffers 214, 216, 218 and 220 therein. (see Fig. 2 of Hadji) The at least one semiconductor storage medium is required to be external in claim 16.

Even if system memory 106 of Hadji were alleged to be external semiconductor storage media, it is not interfaced by a first or a second dedicated bus interface as required in claim 1. Thus, Hadji, or the combination of references cited above, do not describe the additional features set forth in new claim 16.

Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-13 and 15-16 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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